NBTI in GaN MOSFETs: SiO_2 vs. SiO_2/Al_2O_3 gate dielectric

Alex Guo and Jesús A. del Alamo

Microsystems Technology Laboratories (MTL)

Massachusetts Institute of Technology (MIT)

Cambridge, MA, USA

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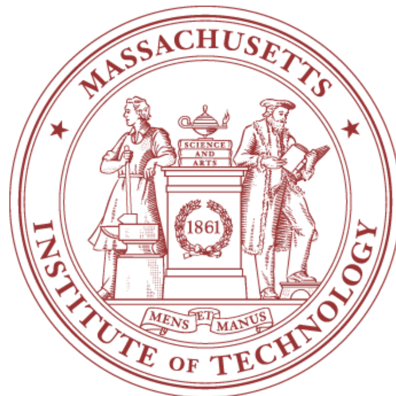

Outline

- Motivation
- Experimental setup
- Results and discussion
- Conclusions

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GaN for power electronics

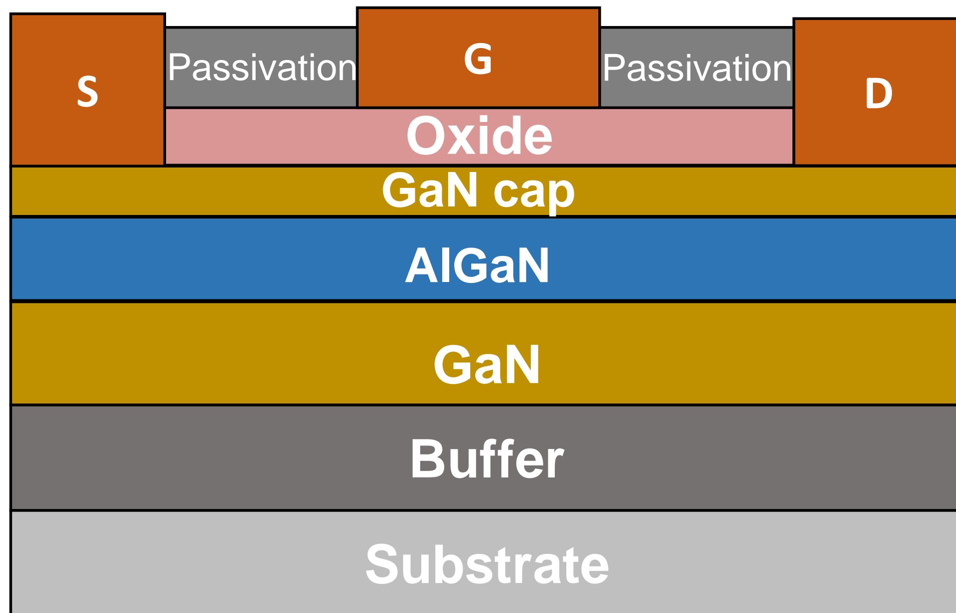
- Promising for a wide range of applications

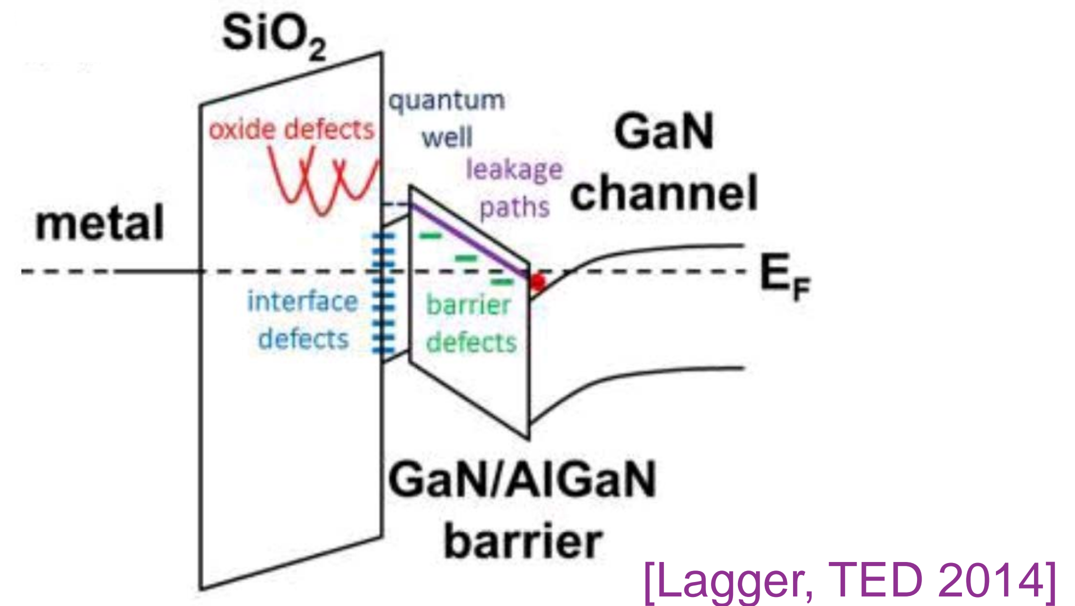
30 V | 600 V | > 1200 V

- Negative-Bias Temperature Instability (NBTI) is a major concern:
  - Operational instability
  - Long-term reliability

GaN MIS-HEMT for high voltage applications

- MIS-HEMT: Metal-Insulator-Semiconductor High Electron Mobility Transistor





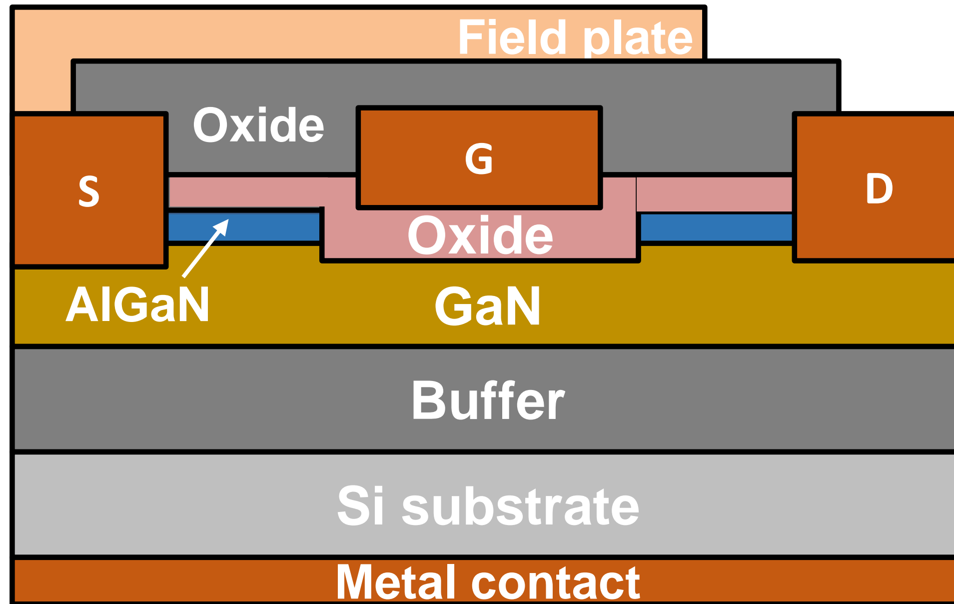
[Lagger, TED 2014]

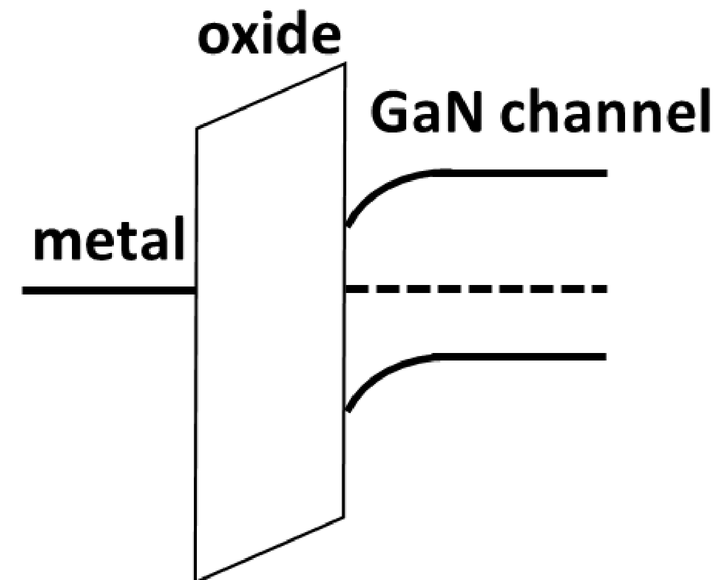
✓ Low gate leakage, large gate swing

x Gate oxide brings stability and reliability concerns not present in HEMTs

This work: simpler GaN MOSFET structure

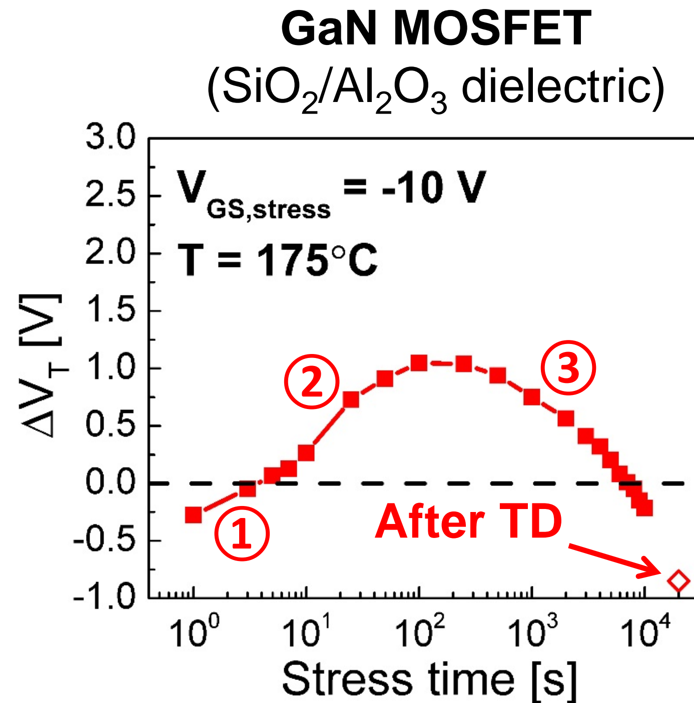
- Industrial prototype devices





- Isolate oxide and oxide/GaN interface
- SiO_2 vs. SiO_2/Al_2O_3 composite, EOT ~ 40 nm

NBTI of GaN MOSFETs



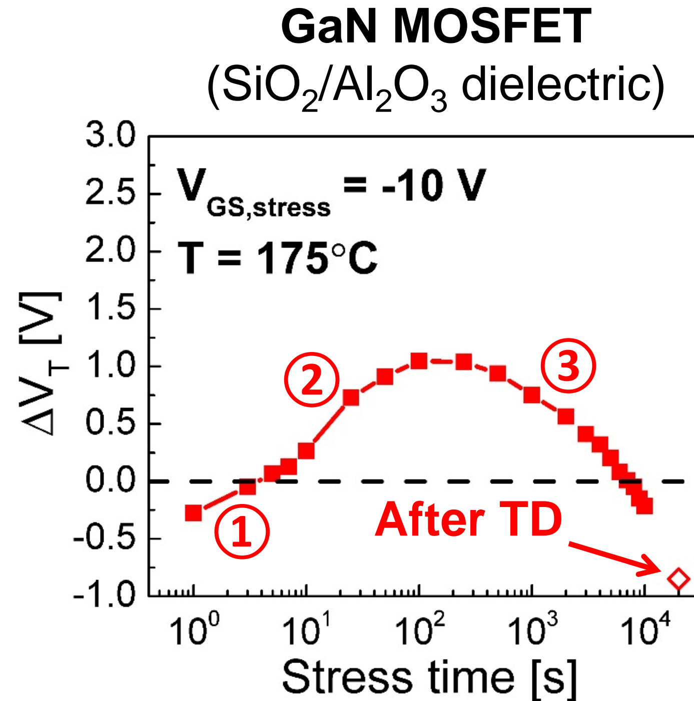
*TD: Thermal Detrapping

[Guo, IRPS 2016]

Three regimes:

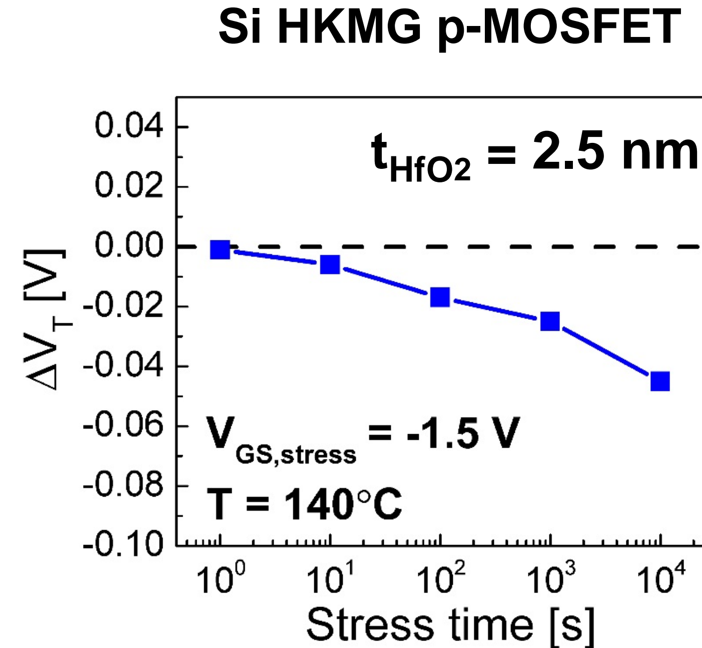
- (Regime 1) Small negative ΔV_T → (regime 2) positive ΔV_T → (regime 3) negative ΔV_T
- Permanent negative ΔV_T after TD

NBTI of GaN MOSFETs



TD: Thermal Detrapping

[Guo, IRPS 2016]

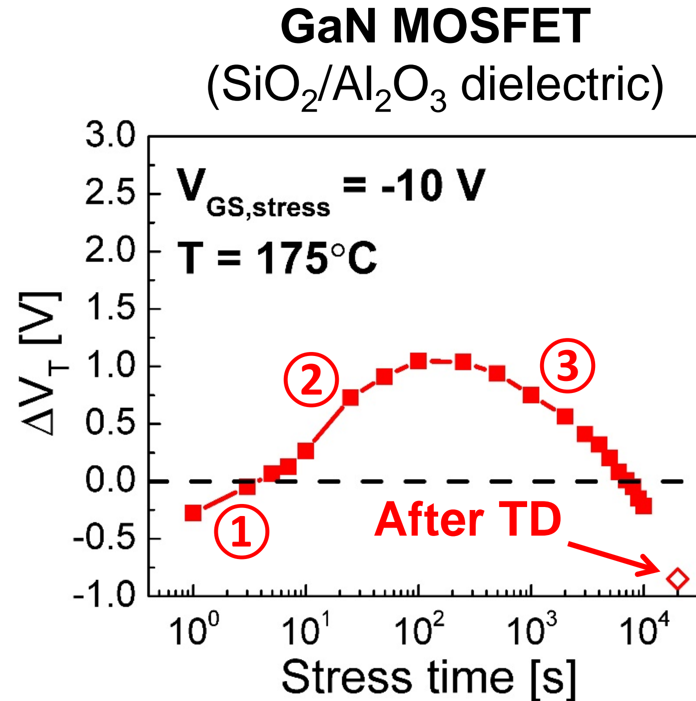


[Zafar, TDMR 2005]

Differences from NBTI of Si HKMG p-MOSFET:

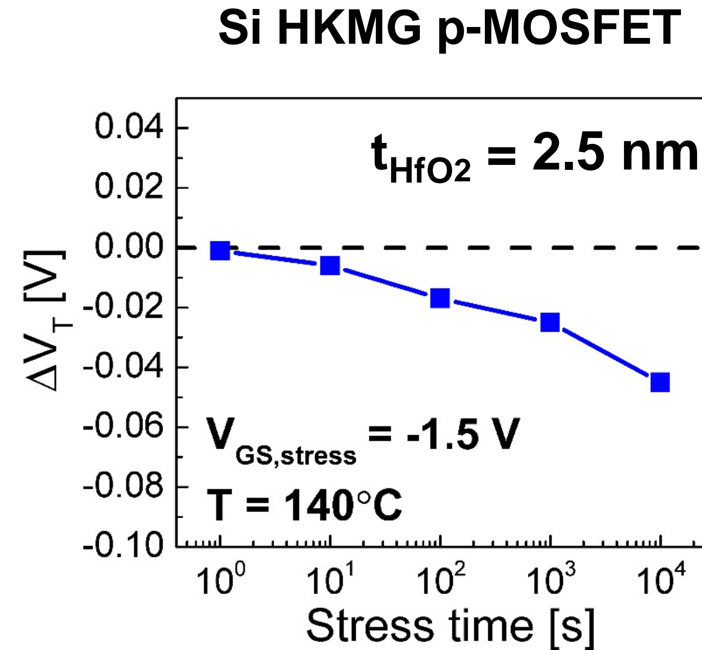
- Larger $|\Delta V_T|$
- Peculiar positive V_T shift in regime 2

NBTI of GaN MOSFETs



TD: Thermal Detrapping

[Guo, IRPS 2016]



[Zafar, TDMR 2005]

Goal of this work: NBTI in SiO_2 vs. SiO_2/Al_2O_3 GaN MOSFETs

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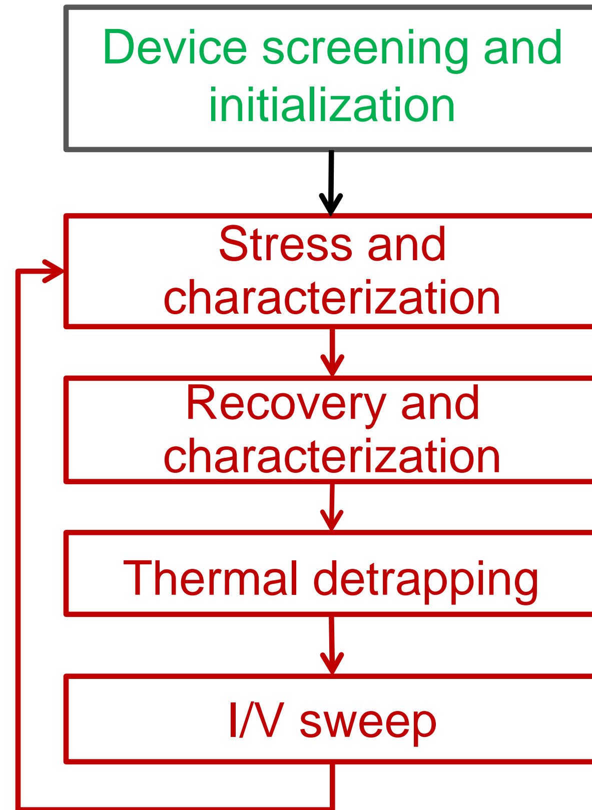
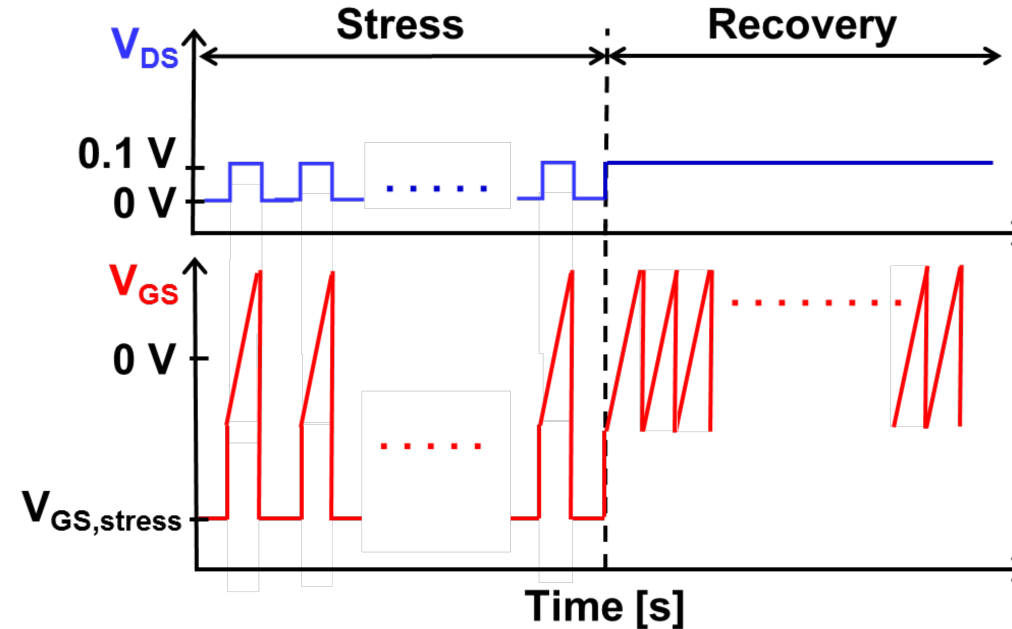
Experimental flow and FOM definition



Increase stress voltage or T



- V_T: V_{GS} value when I_D = 1 μA/mm
- S: Extracted at I_D = 0.1 μA/mm
- $g_{m,max}$: Extracted from I_D-V_{GS} ramp
- All at V_{DS} = 0.1 V
- First sample: ~ 1- 2 s after removal of stress

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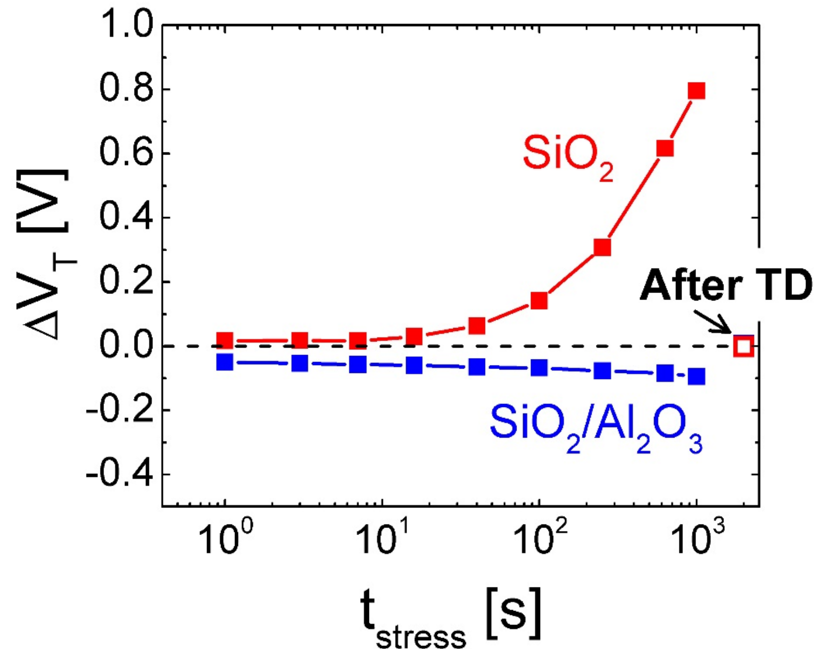
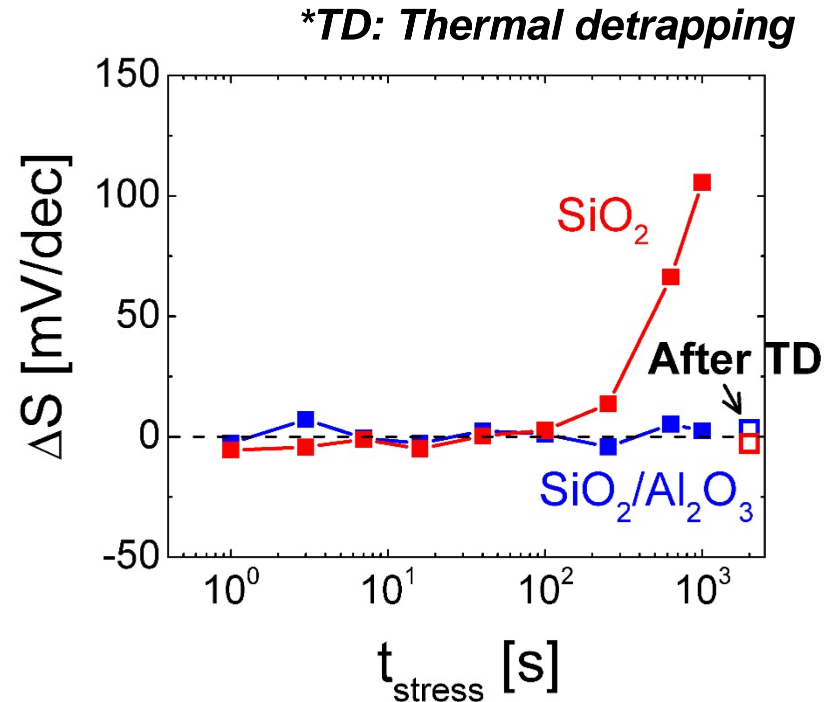
Stress time (t_{stress}) evolution of ΔV_T at RT

- $V_{GS,stress}$ = -2 V (low-stress)

**TD: Thermal detrapping*

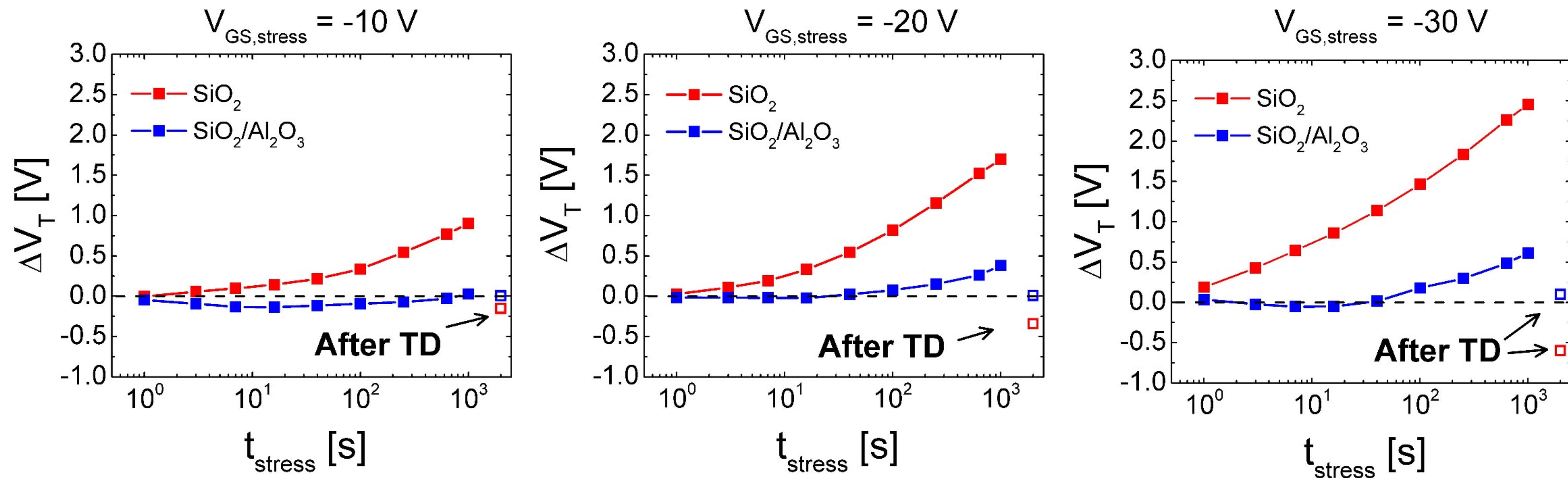




- **SiO_2**: No visible negative ΔV_T; Positive ΔV_T and ΔS for longer t_{stress}; → no regime 1 observed
  SiO_2/Al_2O_3: Negative ΔV_T, negligible ΔS → regime 1
- Both devices completely recovered after TD
  → Lower level of oxide trapping/detrapping in SiO_2 vs. SiO_2/Al_2O_3

Stress time (t_{stress}) evolution of ΔV_T at RT

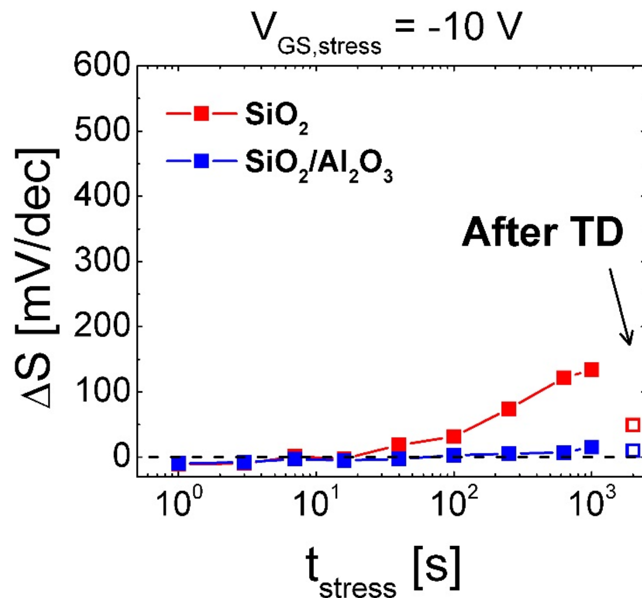
- $V_{GS,stress}$ = -10, -20, -30 V (mid-stress)

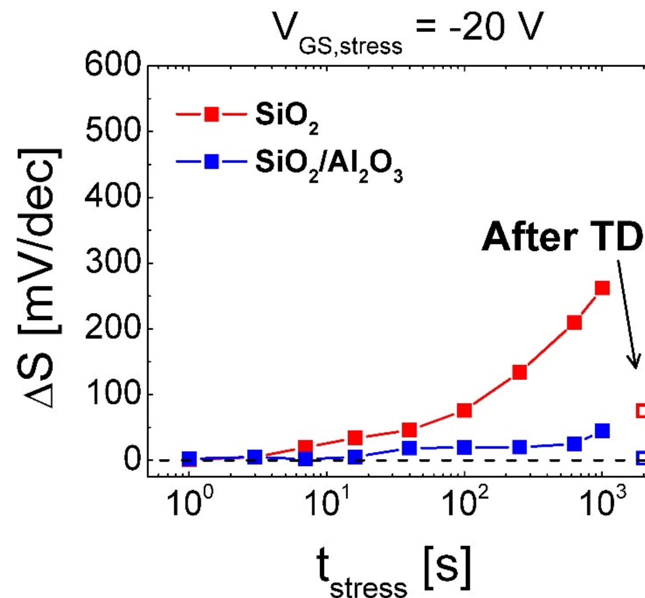


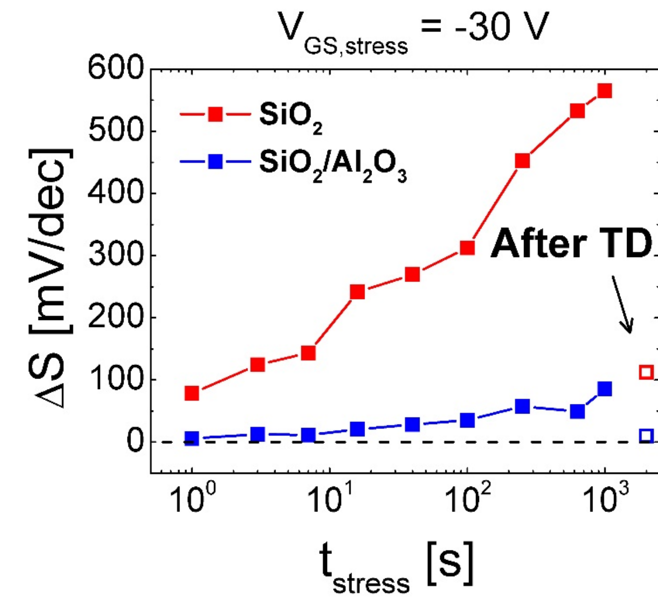
- Positive ΔV_T, both increase with t_{stress} and $V_{GS,stress}$ → regime 2
- SiO_2/Al_2O_3 device completely recovers after TD → regime 2 only
- SiO_2 device shows negative, permanent ΔV_T that increases with $V_{GS,stress}$ → regime 2 + 3

Stress time (t_{stress}) evolution of ΔS at RT

- $V_{GS,stress}$ = -10, -20, -30 V (mid-stress)



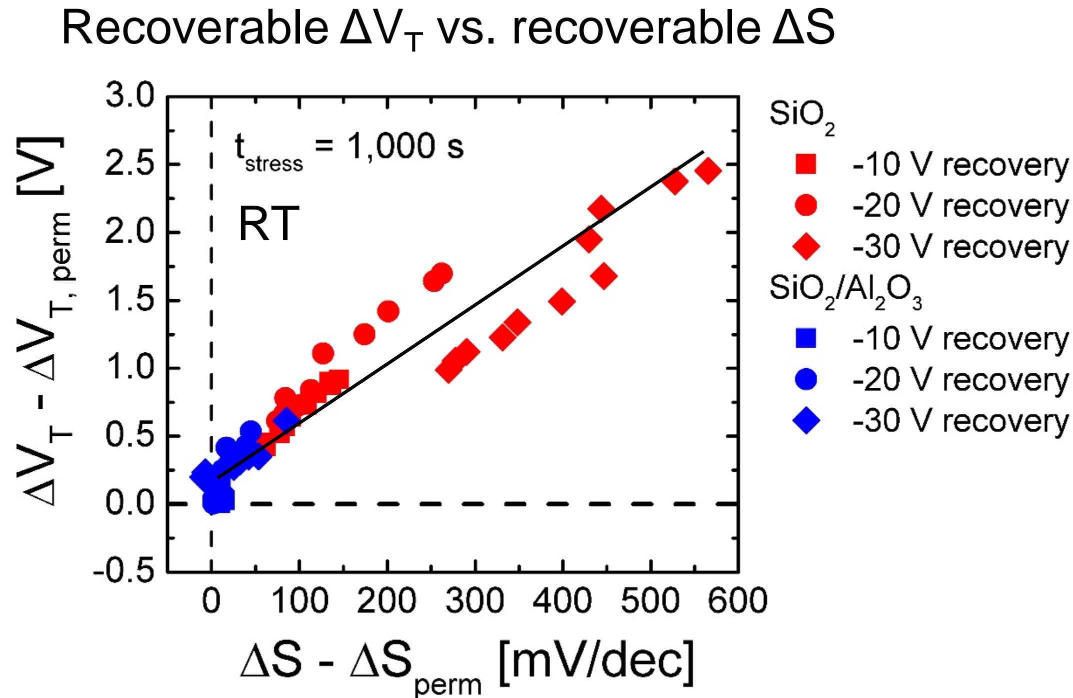


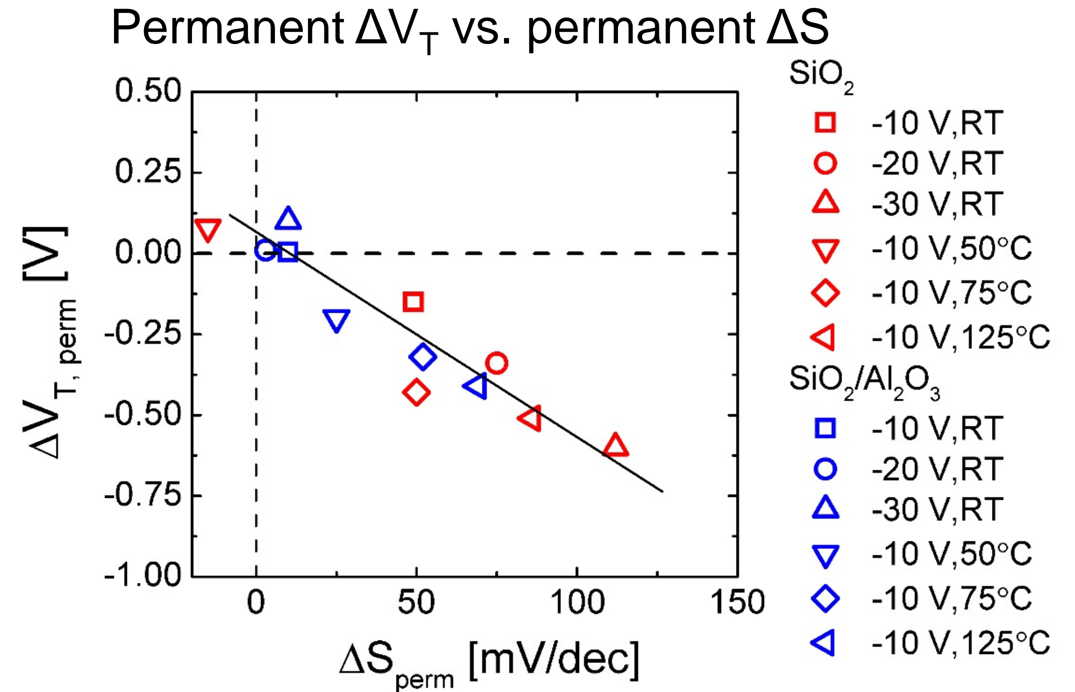


- Positive ΔS increases with t_{stress} and $V_{GS,stress}$ → regime 2
- SiO_2/Al_2O_3 device completely recovers after TD → regime 2 only
- SiO_2 device shows non-recoverable ΔS that increases with $V_{GS,stress}$ → regime 2 + 3

Correlation of ΔV_T and ΔS

- ΔV_T and ΔS correlation after 1000 s stress





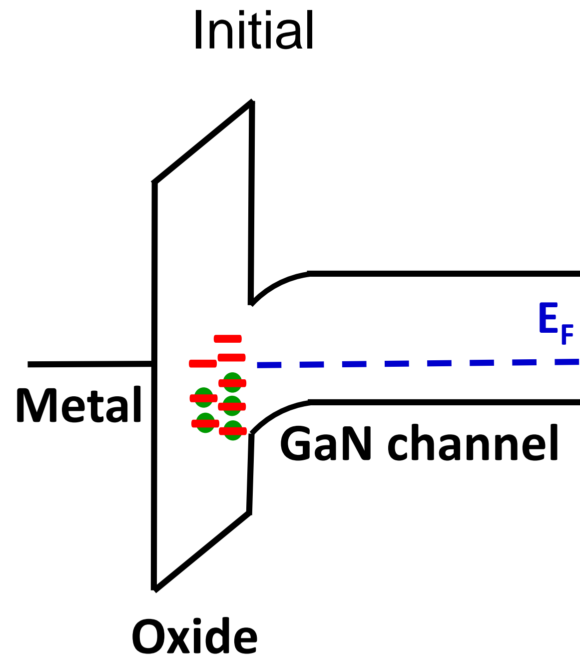
Regime 2:

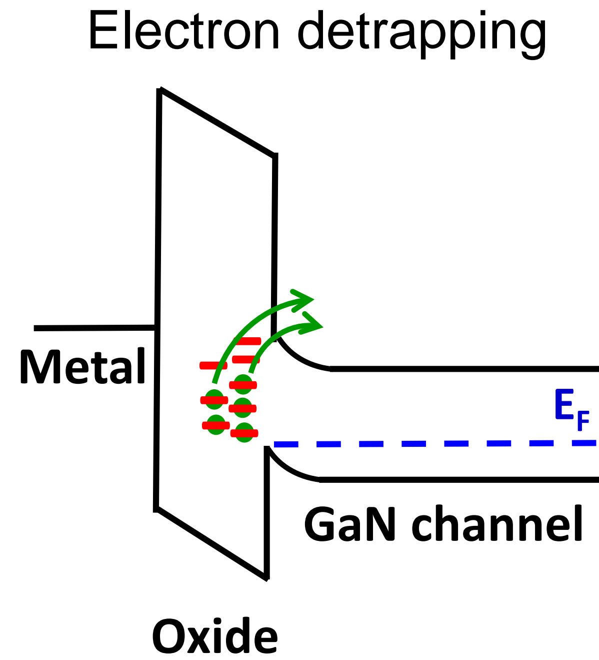
- Recoverable ΔV_T vs. recoverable ΔS linearly correlate
- Suggests same mechanisms

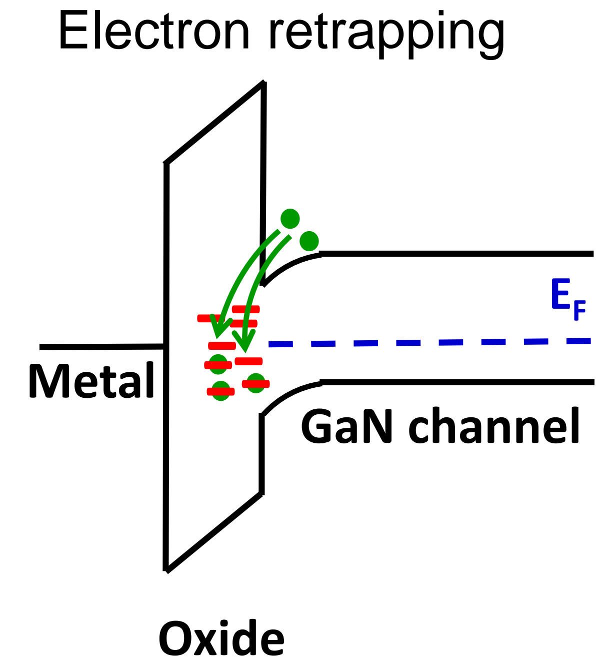
Regime 3:

- Permanent ΔV_T and permeant ΔS linearly correlate
- Suggests same mechanisms

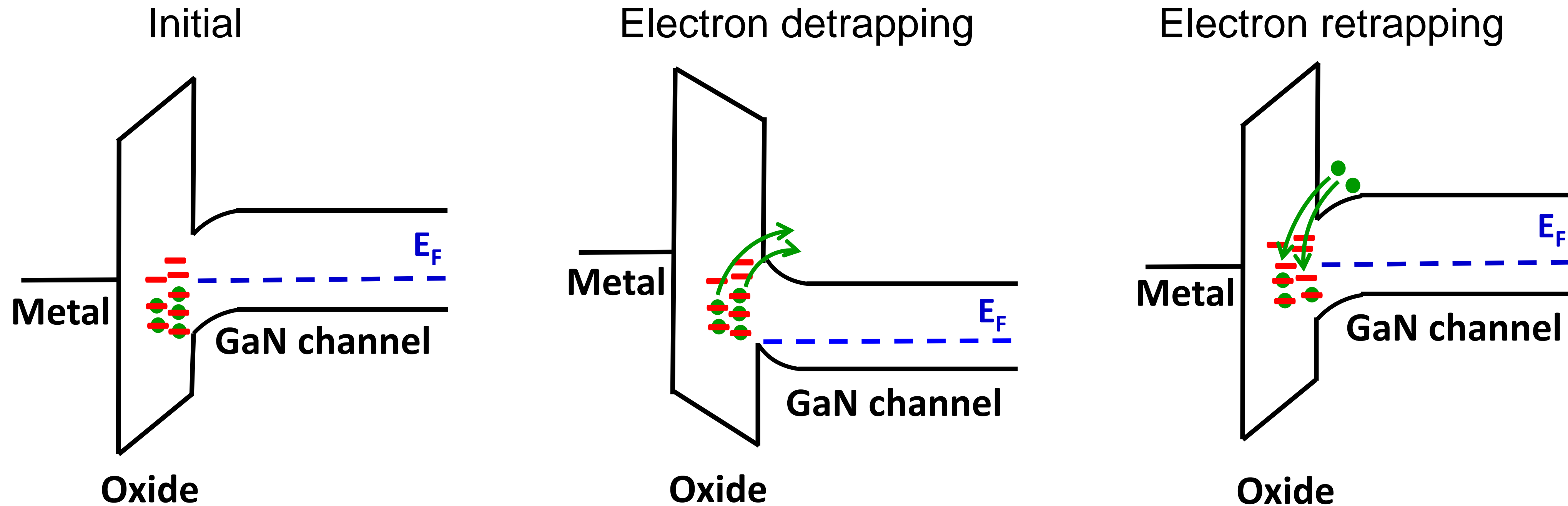
ΔV_T mechanism (regime 1)





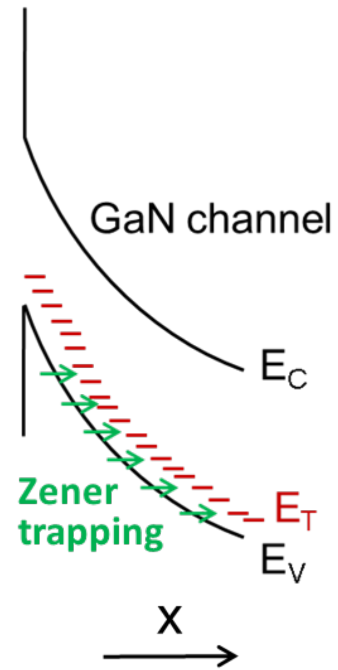


ΔV_T mechanism (regime 1)

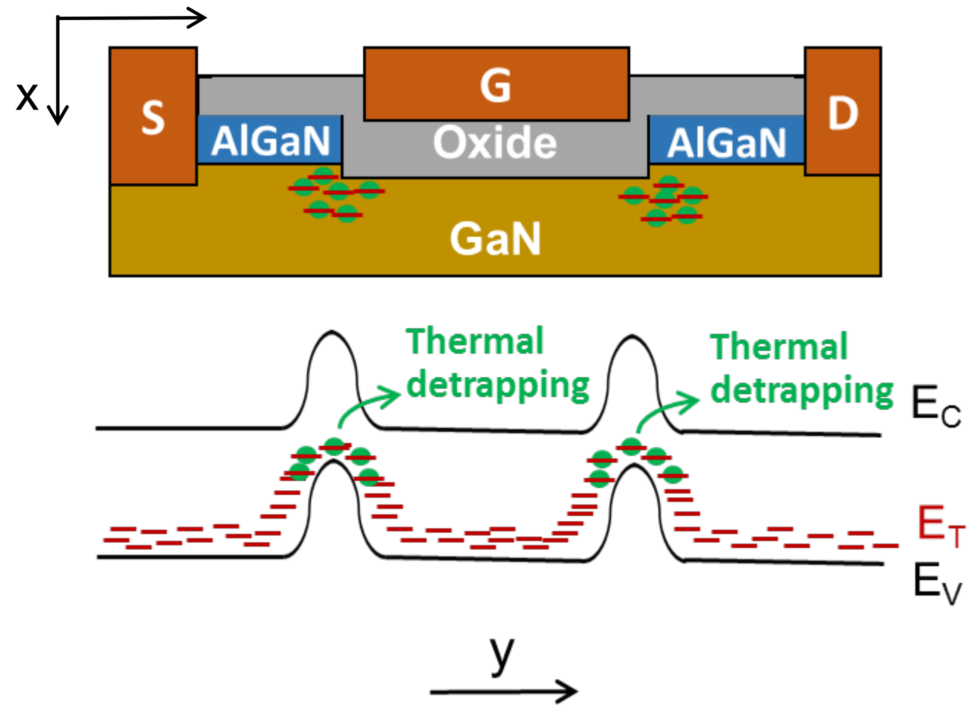


- More prominent electron detrapping in SiO_2/Al_2O_3 devices than in SiO_2 devices
  - → **Border traps in Al_2O_3,** well studied in Si HK system [Jakschik, TED 2004]
  - → Consistent with PBTI study [Guo, IRPS 2015]

ΔV_T mechanism (regime 2)

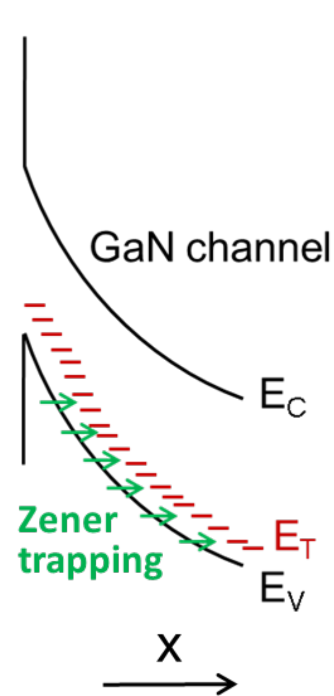


[Jin, IEDM 2013]



[Guo, IRPS 2016]

ΔV_T mechanism (regime 2)



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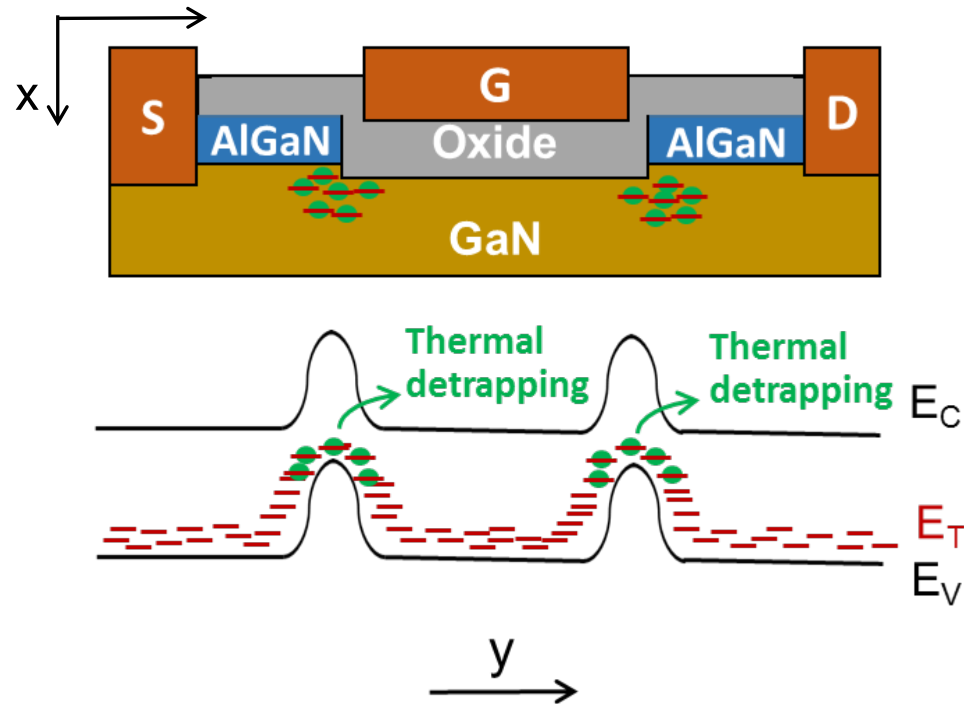
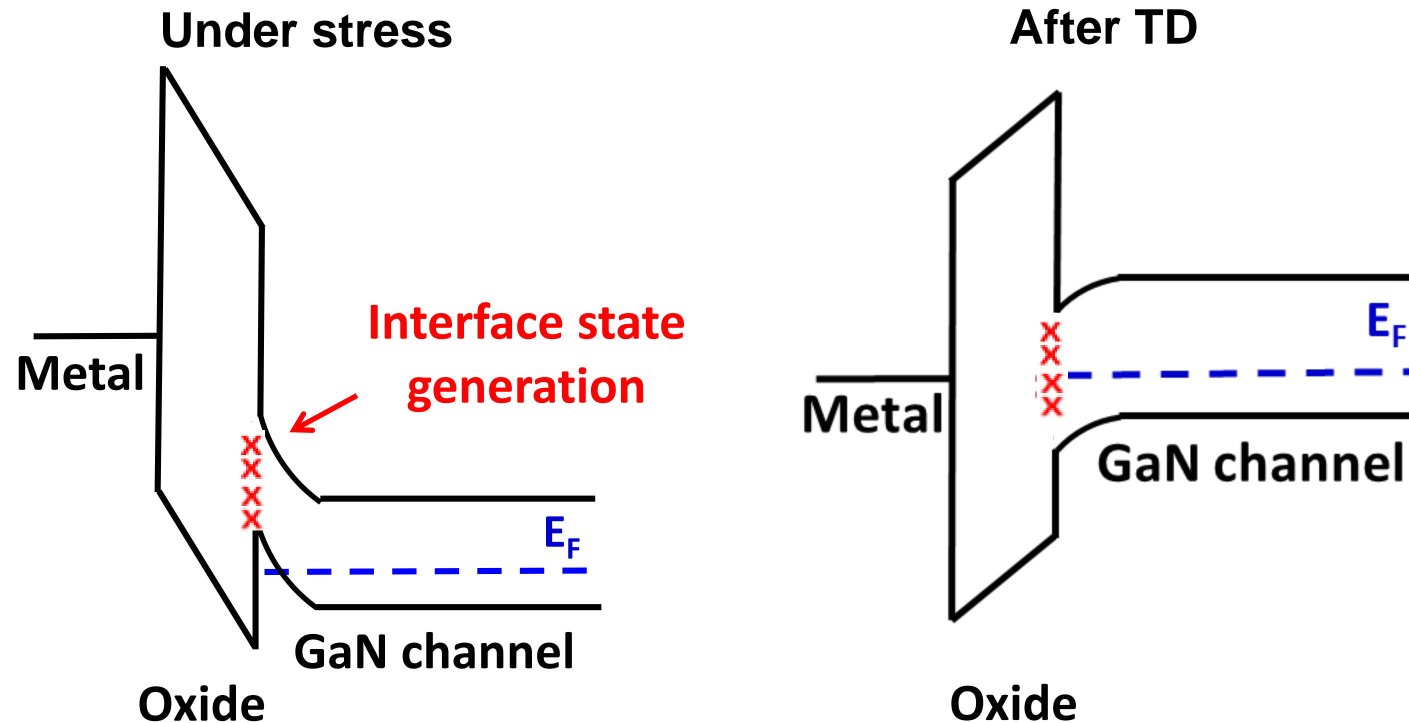


[Guo, IRPS 2016]

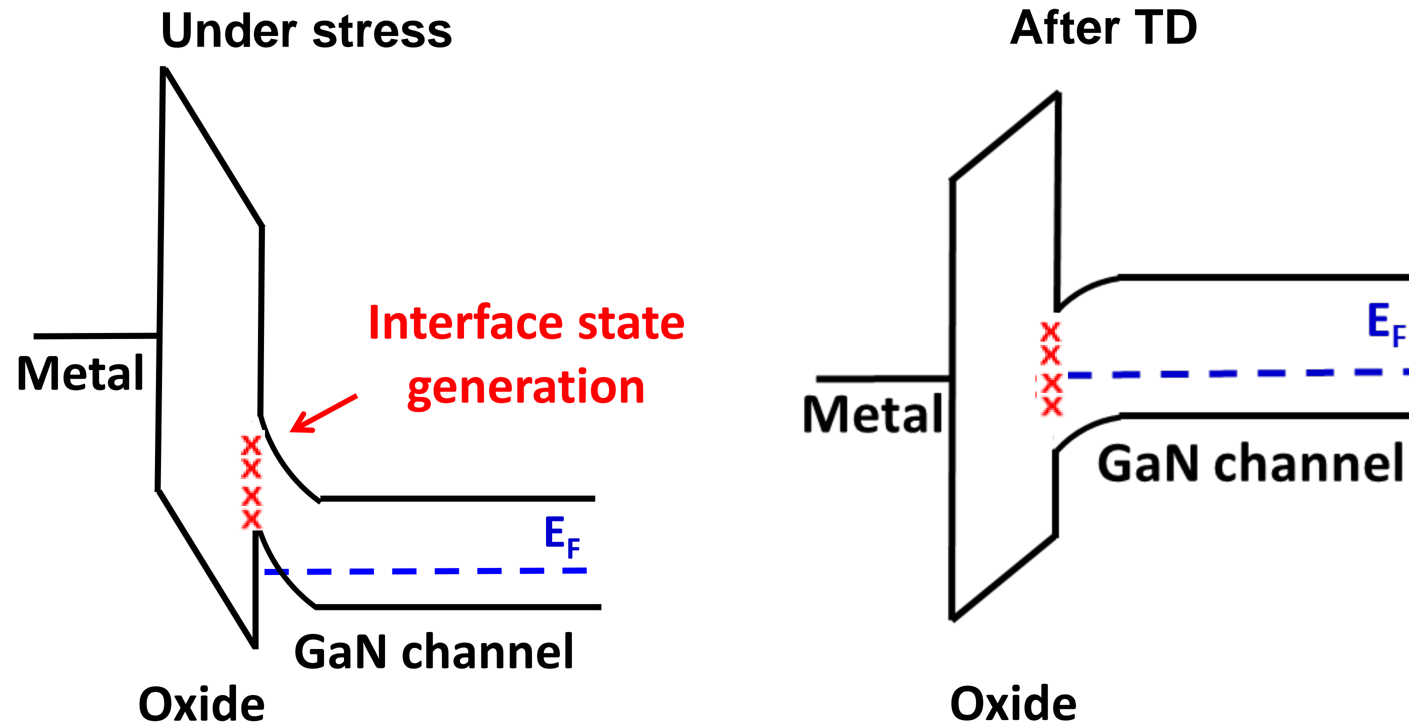
- ΔV_T and ΔS evolution in regime 2 independent of dielectric → consistent with trapping in GaN substrate - more substrate traps in SiO_2 device perhaps due to higher deposition temperature.

ΔV_T mechanism (regime 3)



- Interface state generation under high gate stress, well-studied mechanism in Si MOS system [Schroder, JAP 2007].

ΔV_T mechanism (regime 3)



- Interface state generation under high gate stress, well-studied mechanism in Si MOS system [Schroder, JAP 2007].
- **More severe in SiO_2/GaN interface,** consistent with PBTI study [Guo, IRPS 2015]

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Conclusions

- Understanding of NBTI in SiO_2 vs. SiO_2/Al_2O_3 GaN MOSFETs
  - Regime 1 (low-stress):
    - Electron detrapping from pre-existing oxide traps
    - More prominent in SiO_2/Al_2O_3 due to higher concentration of border traps
  - Regime 2 (mid-stress):
    - Trapping in GaN substrate
    - Greater magnitude in SiO_2 devices, possibly due to defects created during SiO_2 deposition
  - Regime 3 (high-stress):
    - Interface state generation at oxide/GaN interface
    - SiO_2 devices exhibit more fragile interface with GaN (more interface state generation)